EGC220
Class Notes
4/4/2023

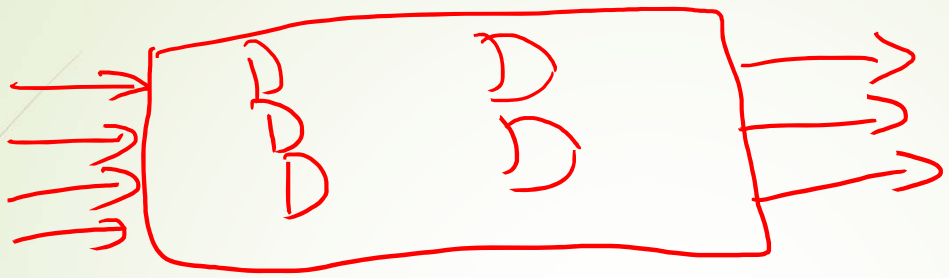
Baback Izadi
Division of Engineering Programs
bai@engr.newpaltz.edu

1. Using Verilog, design an ALU with the following specification:

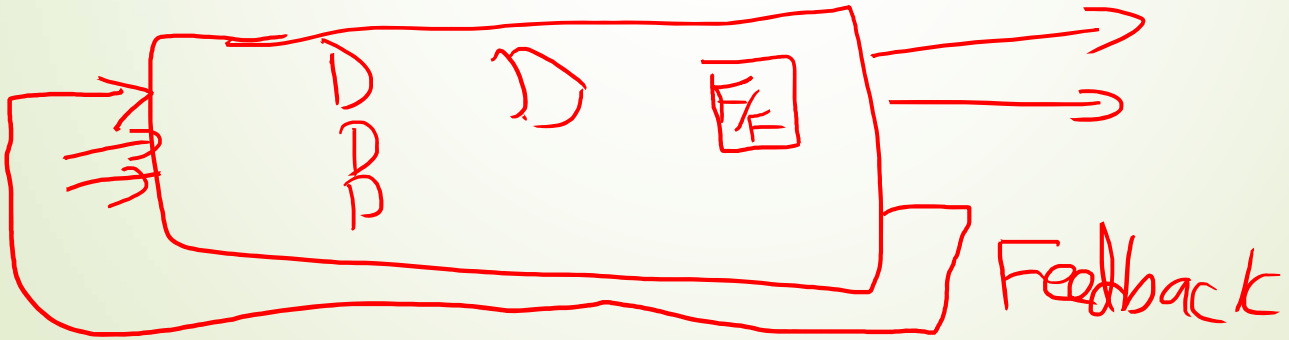
S	Function
0	A-B
1	A+B
2	A + 1
3	A - 1
4	A AND B
5	A OR B
6	A XOR B
7	A’

```
module alu(s, A, B, F);
input [2:0] s;
input [3:0] A, B;
output [3:0] F;
reg [3:0] F;
always @(s or A or B)
case (s)
0: F = A - B;
1: F = A + B;
2: F = A +1;
3: F = A -1;
4: F = A & B;
5: F = A | B;
6: F = A ^ B;
7: F = ~ A;
endcase
endmodule
```

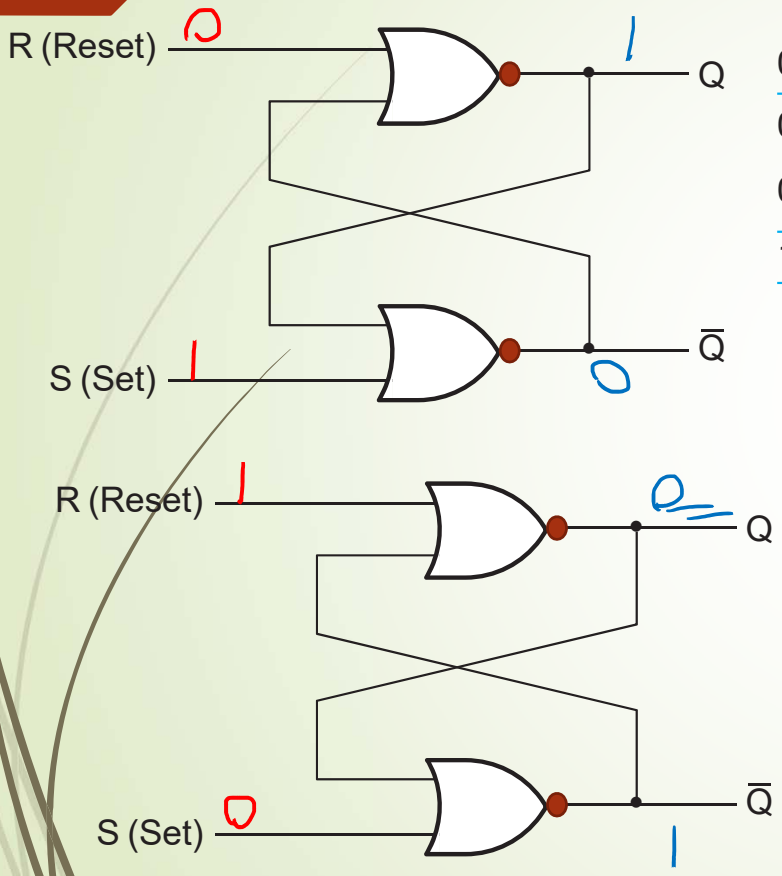
Combinational circuits



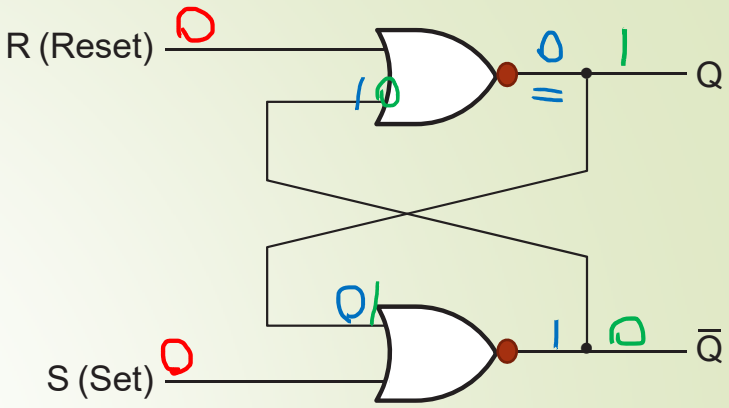
sequential circuits



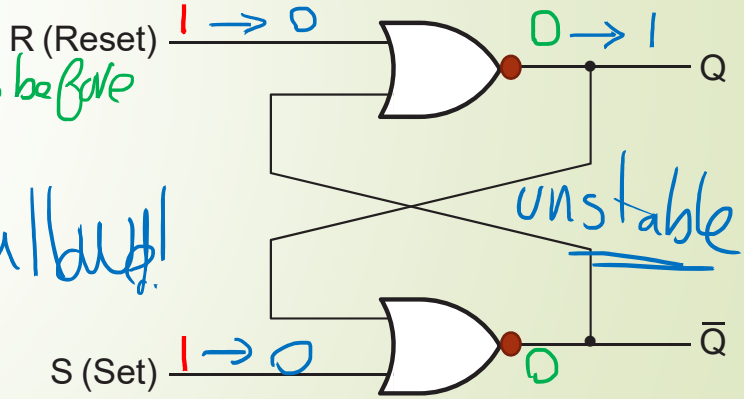
S-R Latch with NOR gates

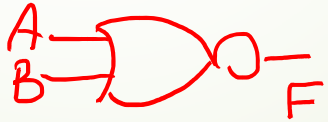


S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined



S	R	Q
0	0	same as before
0	1	0
1	0	1
1	1	Not allowed!

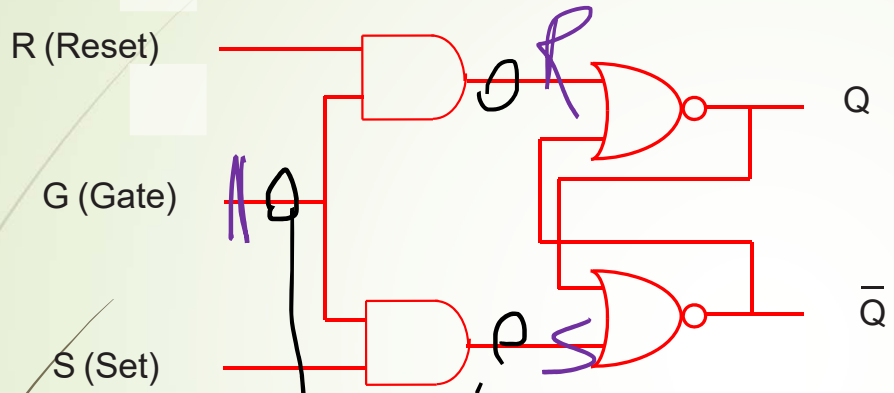




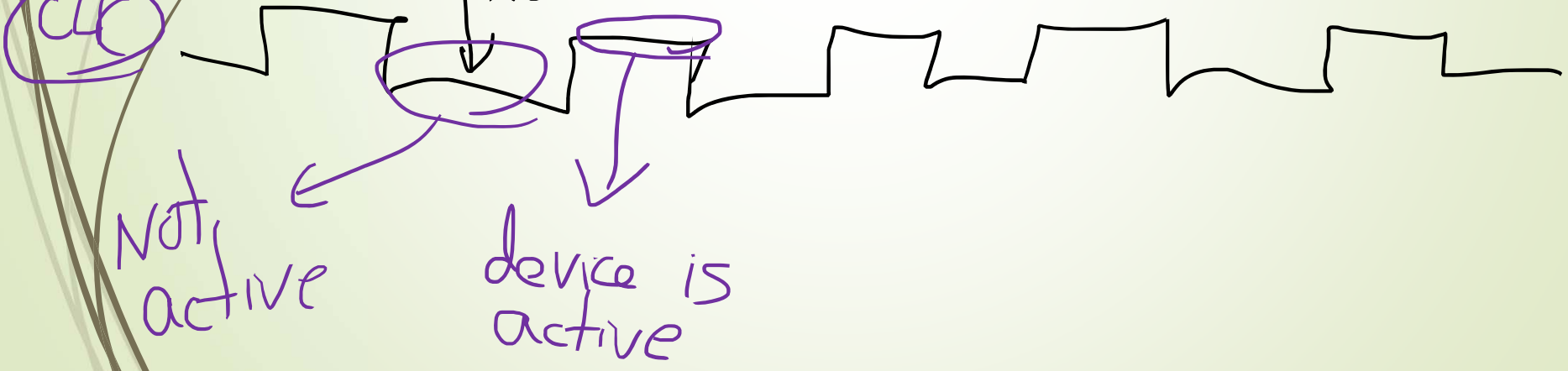
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

→ if one input is 1 output is 0

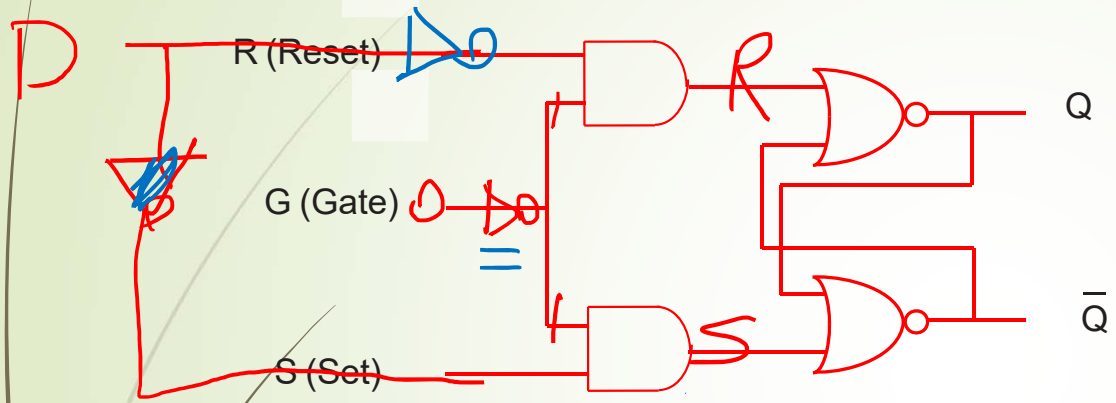
SR Latch

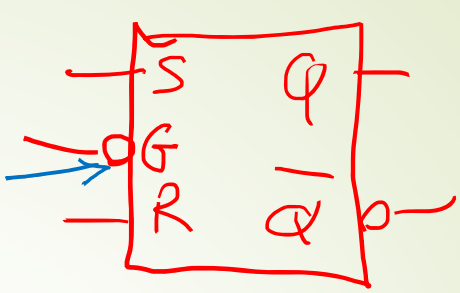


G	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined → not allowed!



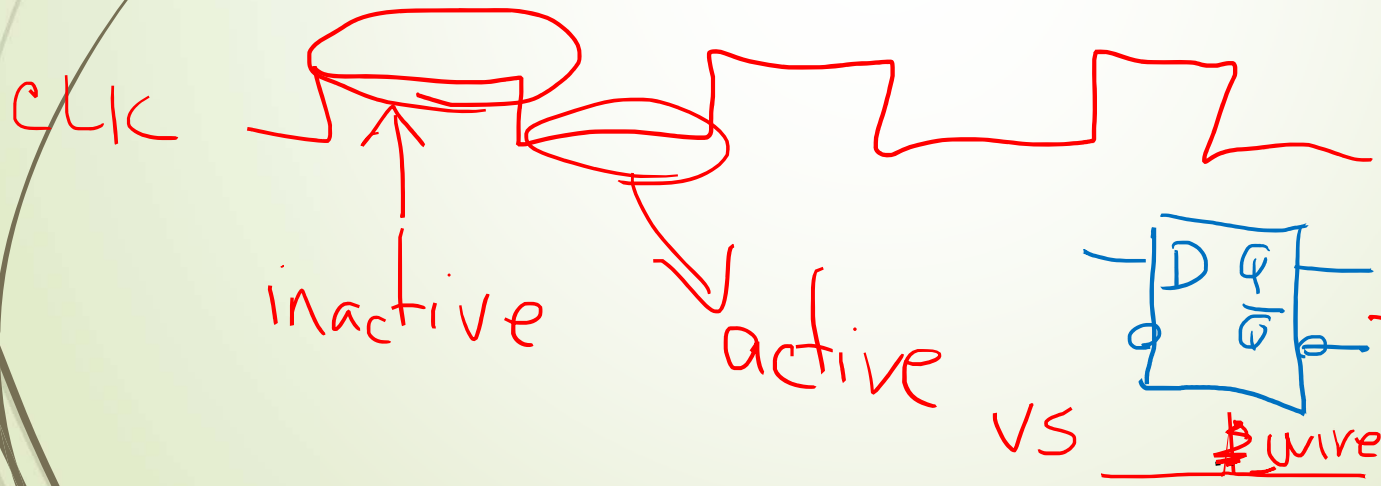
SR Latch





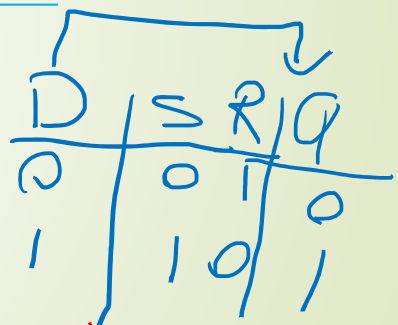
Latch

G	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined



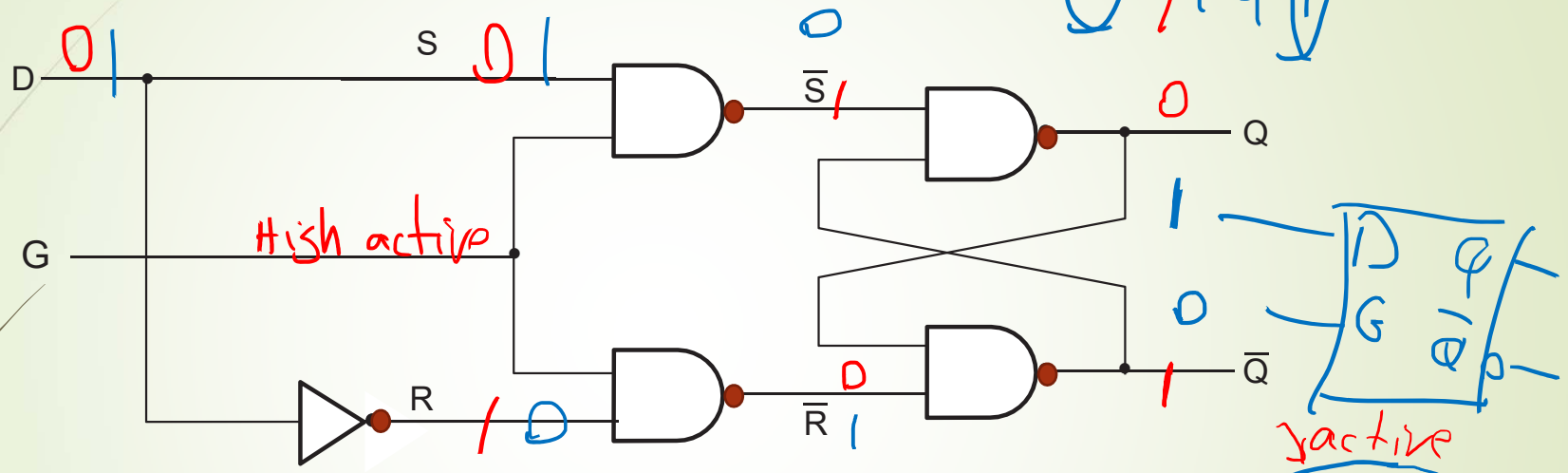
vs

$ wire?



storage device

SR Latch with a Control Gate



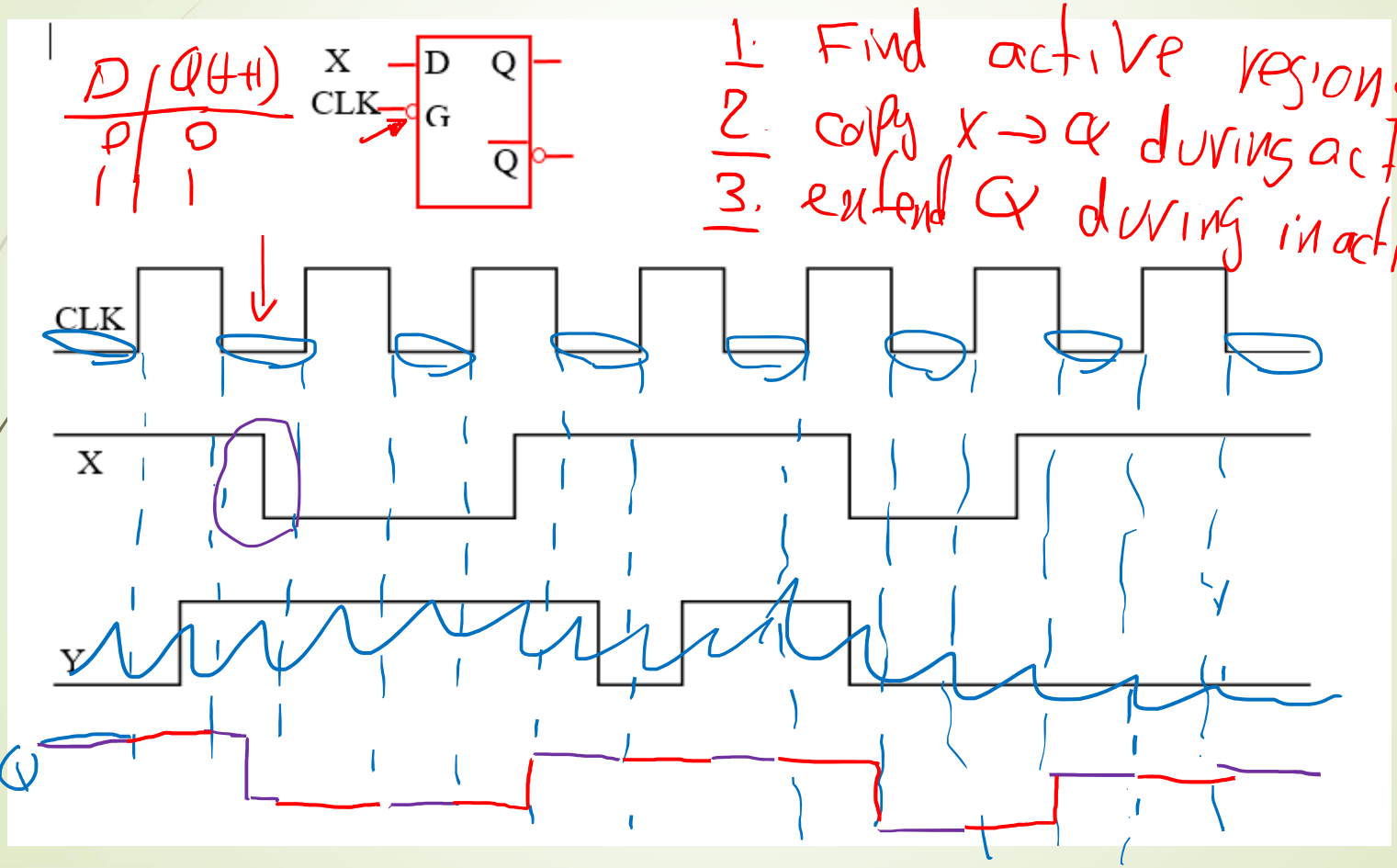
(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

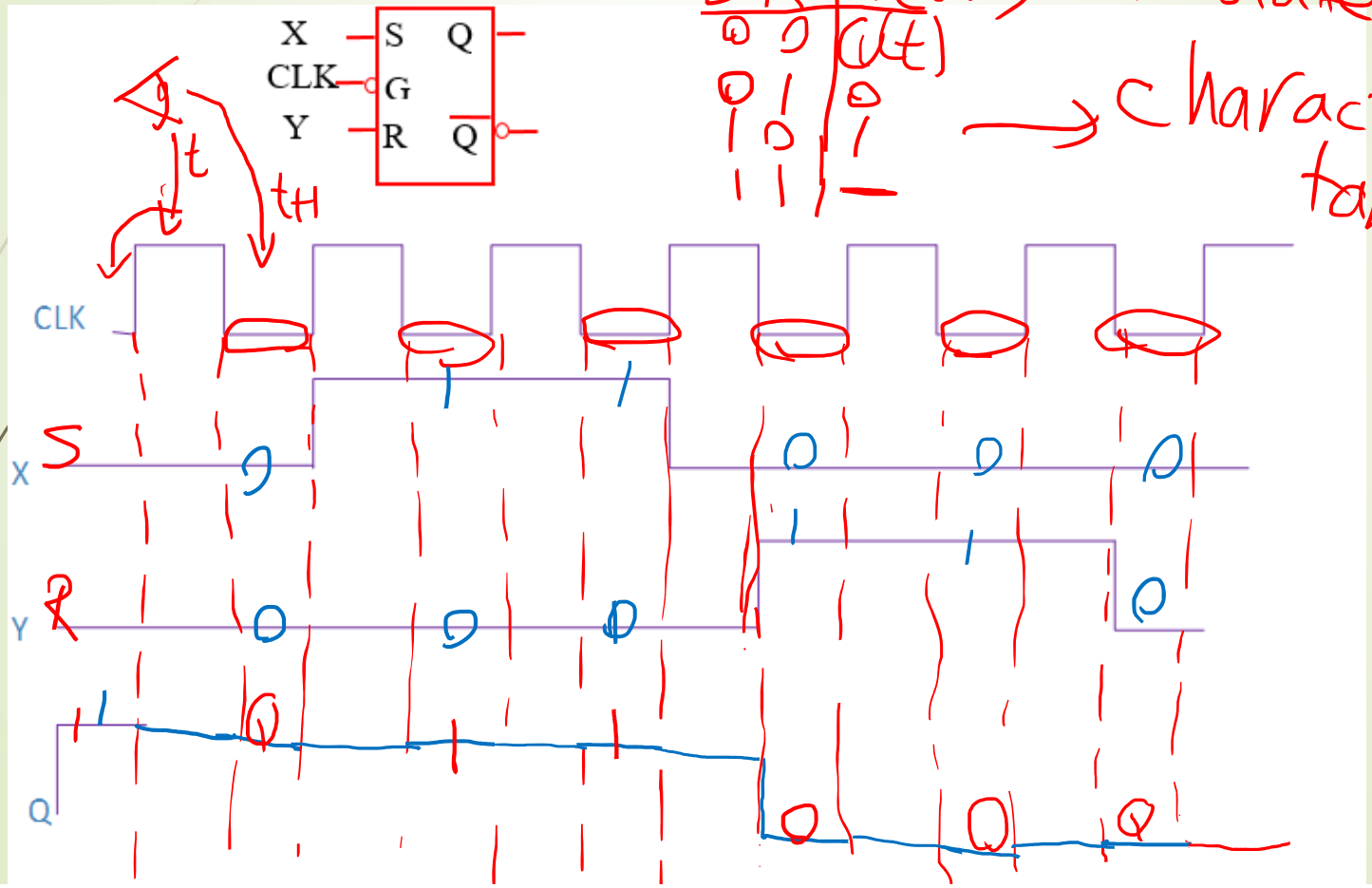
Problem 2

Complete the timing diagram if the following signals are applied as indicated.



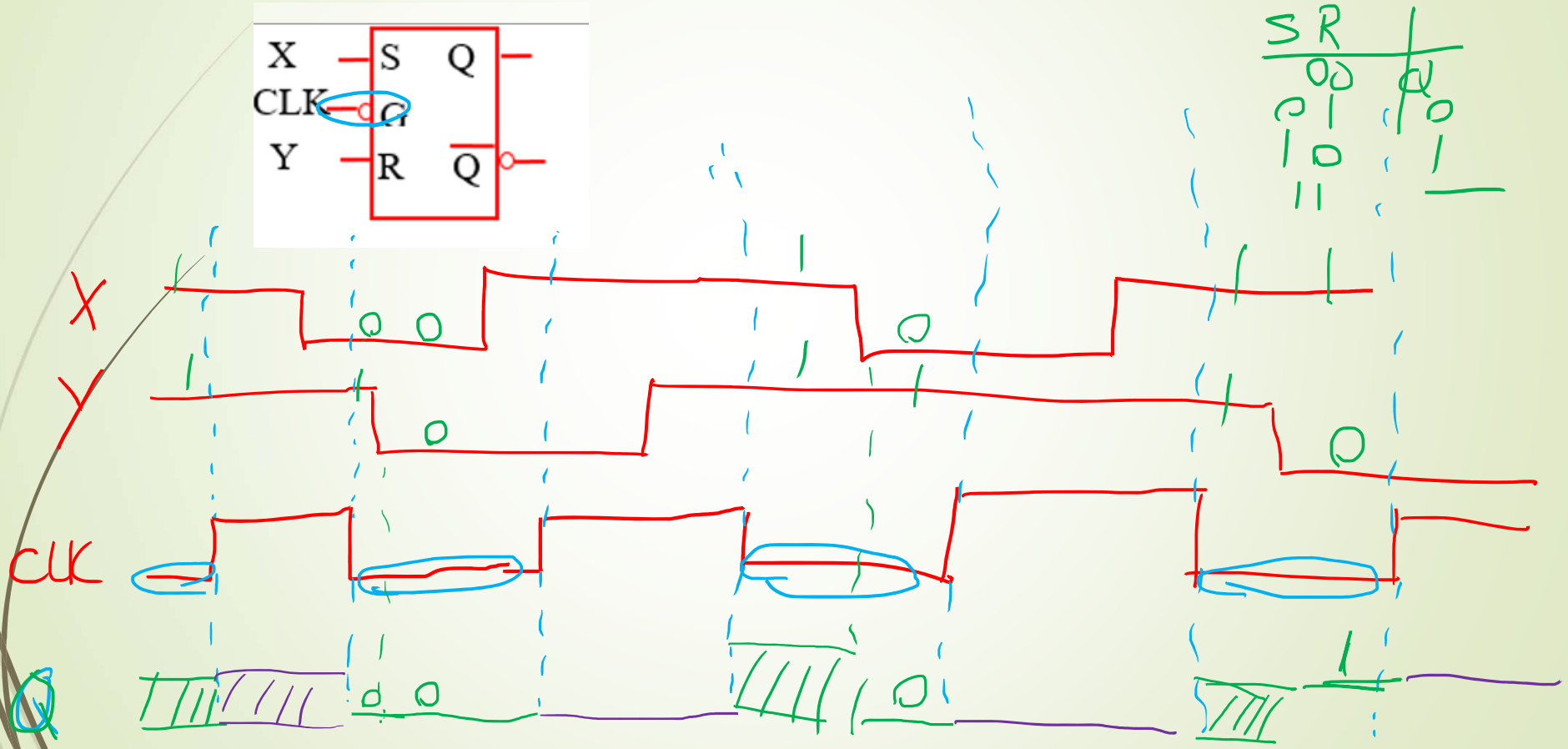
Problem 3

Complete the timing diagram if the following signals are applied as indicated.



Problem

Complete the timing diagram if the following signals are applied as indicated.



Problem 4

Complete the timing diagram if the following signals are applied as indicated.